

**AMENDMENTS TO THE CLAIMS**

The following listing of claims replaces all prior versions and listings.

1-13. (Canceled)

14. (Previously presented) A method for discharging accumulated charge from a body of an SOI device and accessing the SOI device, comprising:

generating a pulse;

using the generated pulse to provide a conductive path from the body of the SOI device to a reference point having a lower potential than the accumulated charge;

discharging the accumulated charge from the body of the SOI device to the reference point;

providing a control signal which enables access to the SOI device; and

reading an output of the SOI device,

wherein said steps of generating a pulse and discharging the accumulated charge occur prior to said step of reading an output of the SOI device.

15. (Previously presented) In a circuit comprising at least one SOI device, a method for enhancing the performance of the circuit, the method comprising the steps of:

providing a pulse discharge circuit connected to the at least one SOI device, said pulse discharge circuit comprising an input signal, a delay element coupled to the input signal and an output signal coupled to the input signal, the output signal driving the circuit; and

using the pulse discharge circuit to discharge any accumulated potential on a body of the at least one SOI device prior to accessing the at least one SOI device.

16. (Previously presented) In a circuit comprising a plurality of SOI devices, wherein said plurality of SOI devices comprises a memory circuit and wherein each of the plurality of SOI devices has a body, a method for enhancing the performance of the circuit, the method comprising:

providing a pulse discharge circuit, the pulse discharge circuit having a pulse generator connected to the circuit;

using the pulse generator to generate a pulse; and

discharging any accumulated potential on the body of at least one of the plurality of SOI devices to a point having a lower potential than the accumulated potential of the body in response to the pulse from the pulse generator just prior to accessing the memory circuit for reading or writing data.